1. A method comprising:

forming a damascene via to a conductive line in the periphery of a phase change memory.

2. The method of claim 1 including forming a phase change memory including a phase change storage element and a phase change threshold switch.

3. The method of claim 2 including forming said switch over said element.

4. The method of claim 3 including forming a pore over a substrate, said pore having a dimension smaller than the feature size possible with available lithographic techniques.

5. The method of claim 4 including forming said pore by forming an aperture through an insulator and forming a sidewall spacer in said aperture.

6. The method of claim 5 including forming the lower electrode of said phase change storage element in said pore.

7. The method of claim 2 including forming a barrier layer between said threshold switch and said storage element.

8. The method of claim 1 including forming an upper electrode that has a vertical extent at least twice its horizontal extent.

9. The method of claim 2 including forming an upper electrode over said phase change storage element and said threshold switch, said electrode having sidewall spacers.

10. The method of claim 9 including using said sidewall spacers as a mask to etch through underlying layers.

11. The method of claim 1 including forming a plurality of cells as a plurality of integrated islands spaced from one another.

12. The method of claim 11 including filling the regions surrounding said islands with an insulator.

13. The method of claim 12 including forming said insulator to a height over the upper extent of said upper electrodes.

14. The method of claim 13 including forming grooves through said insulator down to and past the upper extent of said upper electrodes.

15. The method of claim 13 including forming a vertical groove in a memory array and a periphery.

16. The method of claim 15 including filling said groove in said periphery with a sacrificial light absorbing material.

17. The method of claim 16 including etching said groove in said periphery into said sacrificial light absorbing material.

18. The method of claim 17 wherein forming a damascene via includes filling said grooves with a conductive material.

19. The method of claim 18 including forming said groove in said periphery deeper than said grooves in the memory array.

20. The method of claim 19 including forming said grooves in said periphery to a depth below the upper extent of said upper electrode and above the lower extent of said upper electrode.

21. An apparatus comprising:

a phase change material;

a conductive line coupled to said phase change material; and

a damascene via to said conductive line.

22. The memory of claim 21 wherein said memory includes a phase change storage element and a phase change threshold switch.

23. The memory of claim 22 wherein said switch is formed over said element.

24. The memory of claim 23 including a substrate, a pore over said substrate, said pore having a dimension smaller than the feature size possible with available lithographic techniques.

25. The memory of claim 24 including an insulator over said substrate, said pore formed as an aperture in said insulator, said pore having a sidewall spacer in said aperture.

26. The memory of claim 25 including an electrode for said phase change storage element in said pore.

27. The memory of claim 22 including a barrier layer between said threshold switch and said storage element.

28. The memory of claim 21 including an upper electrode having a vertical extent at least twice its horizontal extent.

29. The memory of claim 21 wherein said damascene via includes a metal line extending through an insulator.

30. A system comprising:

a controller;

a wireless interface coupled to said processor-based device; and

a memory coupled to said device, said memory including a phase change material, a conductive line coupled to said phase change material, and a damascene via to said conductive line.

31. The system of claim 30 wherein said memory includes a phase change storage element and a phase change threshold switch.

32. The system of claim 31 wherein said switch is formed over said element.

33. The system of claim 32 including a substrate, said pore over said substrate, said pore having a dimension smaller than the feature size possible with available lithographic techniques.

34. The system of claim 33 including an insulator over said substrate, said pore formed as an aperture in said insulator, said pore having a sidewall spacer in said aperture.

35. The system of claim 34 including an electrode for said phase change storage element in said pore.

36. The system of claim 30 wherein said wireless interface includes a dipole antenna.